

TAPERED DELAY LINE

BACKGROUND OF THE INVENTION

The present invention relates to thin film delay lines and, in particular, to resistive, thin film circuit devices defined by symmetrical patterns containing conductive pathways of non-uniform width and spacing between adjacent conductors.

Varieties of thin film devices have been constructed for high frequency circuits. Most have been directed to microwave applications. Some devices, such as discrete delay line assemblies, have been constructed for higher frequency applications.

Delay lines are frequently used to adjust timing inconsistencies at complex circuitry mounted to complex printed circuit boards that operate at ever increasing higher frequencies. Desirably therefore any delay line should accommodate these higher frequency applications by exhibiting a constant impedance over the operating delay period. Secondly, it is desirable that the devices can be produced at reduced sizes. Examples of some discrete, multi-layer, delay line devices constructed on ceramic substrates are shown at US patents 5,030,931; 5,365,203; and 5,499,442.

The subject invention provides patterned thin film devices wherein the inductive and capacitive characteristics of the conductors that define the device are tailored by varying the line width and line spacing between adjacent conductors over the device. Several delay line circuits having a nominal 50 ohm impedance characteristic are disclosed wherein non-uniformities are formed in regions of the conductors that are not bordered on both sides by adjoining conductors, that is at the input or outermost and output or innermost conductors of a spiral patterned delay line. A reduced inductance of narrowed conductors is particularly offset with narrowed line spacing to reduce the

capacitance and whereby the operating Z_0 of the delay lines is improved. Several alternative coil or spiral arrangements that exhibit different delays are disclosed that are constructed on rigid and flexible dielectric substrates. Necessary terminations are connected with solder filled vias and/or edge connections to the rigid or flexible substrate.

SUMMARY OF THE INVENTION

It is a primary object of the present invention to provide thin film devices having conductors of non-uniform line width and spacing between adjacent conductors to control the inductive and capacitive characteristics of the device.

It is a further object of the invention to provide thin film devices constructed from symmetrical conductor patterns, such as zigzag, serpentine, spiral or coil shapes, wherein regions of the conductors are formed with non-uniform line width and spacing between adjacent conductors to control the inductive-capacitive characteristics of the device.

It is a further object of the invention to provide alternative delay line circuits constructed from one or more coil shaped paths wherein the innermost and/or outermost conductors exhibit reduced or wider line widths and/or narrowed line spacing from other adjoining conductors.

It is a further object of the invention to provide a device with conductors of tailored shape and a ground plane of tailored thickness.

Various of the foregoing objects, advantages and distinctions of the invention can be found in alternative thin film delay line devices and circuits constructed on rigid and flexible/foldable ceramic substrates. Several coil shaped delay lines having a nominal 50 ohm impedance characteristic are defined by conductors of varying the line width and

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line spacing between adjacent conductors over the device. The conductor non-uniformities are formed in regions of the conductors that are not bordered on both sides by adjoining conductors.

Still other objects, advantages and distinctions of the invention will become more apparent from the following description with respect to the appended drawings. To the extent alternative constructions, improvements or modifications have been considered they are described as appropriate. The description should not be literally construed in limitation of the invention. Rather, the scope of the invention should be broadly interpreted within the scope of the further appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Like reference numerals refer to like structure at the various drawings and which are as follows:

Figure 1 is a diagram of a typical "prior art" thin film delay line.

Figure 2 is a diagram of a 0.9nsec tapered delay line.

Figure 3 is a diagram of a 1.8 nsec tapered delay line.

Figure 4 is a diagram of a 4.25 nsec folding, tapered delay line.

Figure 5 shows an exemplary signal waveform for a delay line device of Figure 4 in solid line relative to a similar device (shown in dashed line) having a conventional conductor pattern of geometrically identical shape but wherein all conductive paths exhibit the same width and inter-conductor spacing.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Figure 1, a typical prior art delay line device 2 is shown. The device 2 is defined by a patterned, conductive signal path 4 having a number of zig-zag or

serpentine convolutions 6 that are symmetric with respect to each other. Each convolution 6 includes a linear portion 8 that extends parallel to an adjoining neighbor and is constructed using conventional thin film processes as distinguished from integrated circuit processes. The width of each convolution 6 is the same as the others and the spacing between each linear portion 8 is the same.

The electrically conductive signal path 4 is defined by a thin film that is deposited and patterned using conventional plating, sputtering, cvp deposition or the like and compatible photolithography and etching techniques to derive the conductive path 4. It is to be appreciated the path 4 can take myriad forms wherein the conductors wind back and forth upon each other. Each convolution 6 can also include several sub-convoluted paths and the pattern of which are repeated.

The patterned signal path 4 is constructed on a top surface of a dielectric substrate 10, for example, a resin board, ceramic oxide, zirconia-tin-titanate or other material having a desirable dielectric characteristic. A suitable ground plane 12 is deposited on the bottom surface of the substrate 10.

The time delay T_d of the device 2 is a function of the self and mutual inductance of the conductive paths 8 and the parallel plate and fringe capacitance between the several adjoining conductive paths 8 and ground plane 12, that is, $T_d = \sqrt{LxC}$. At operating frequencies in excess of 200 MHz, the impedance (Z_o) characteristic of the device varies over time, since the inductance contributed by the outermost end conductors 14 and 16 is relatively less than the inner conductors. That is, there are fewer adjoining conductors to couple with at the input and output ends and therefore less mutual inductance. Signal artifacts thus appear when measuring the impedance

characteristic of the device. At the relatively high operating frequencies at which delay lines are now commonly implemented, the spurious signal artifacts can affect the performance of the principal circuitry with which the delay line is coupled.

Because it is desirable to maintain a constant impedance Z_0 during the entire period of the time delay and appreciating that $Z_0 = \sqrt{L/C}$, attempts have been made to reduce the spacing between relatively unbounded or uncoupled conductors of circuits having uniform conductor widths. Other attempts have been directed to reduce the inductance and line width of uncoupled conductors and simultaneously reduce the capacitance of the uncoupled conductors to offset the reduced inductance to maintain Z_0 .

In the latter regard, the outermost and innermost conductors of the coil shaped delay line circuits 20, 30 and 40 of Figures 2-4 have been modified at the input and output ends. That is, the line width of the outermost, input end and innermost, output end conductors have been reduced and the spacing relative to the nearest adjoining conductor has been reduced. Device performance has thereby been improved (i.e. a relatively smoother impedance Z_0 characteristic is created) as exemplified by the comparative waveforms shown at Figure 5 for the device 40.

Figure 5 particularly exemplifies the impedance characteristic exhibited by a test signal impressed on two nominal 2.0 nanosecond delay lines. The signal shown in dashed line is that of a delay line constructed in conventional fashion with conductors of uniform line width and line spacing. The solid line signal is exhibited by a delay line of identical pattern but constructed with the improved (i.e. tailored line shape/line spacing) conductors of the devices 20, 30 and 40 of Figures 2-4. Figure 5 demonstrates the

relatively smoother impedance characteristic and reduced peak-to-peak swing of Z_0 that is obtained by tailoring the conductors.

Each of the improved devices of Figures 2-4 provides non-uniform line width and line spacing at the outermost (input end) and innermost (output end) conductor coils and coupling conductors. With attention to Figure 2, the device 20 provides a square coil shaped conductive path 22 wherein the interior coils 27, 27' and 27'' are each sized at a nominal 0.240 inch line width and a 0.160 inch spacing between the interior coils 27, 27' and 27''. Relatively thinner outermost and innermost conductors 24 and 25 are formed with a nominal 0.060-inch line width and a 0.080-inch spacing between the coils 24-27 and 25-27''. The reduced capacitance exhibited by the conductors 24, 25 and 26 offsets the comparatively low inductance of the uncoupled conductors 24 and 25 such that the device 20 exhibits a substantially uniform 50-ohm impedance to signals coupled to the device 20. The line width and/or line spacing of the device conductors wherever they are uncoupled from other parallel conductors. It may also be desirable to tailor the thickness of the ground plane 12 in the regions of a device's coupled and uncoupled conductors to control the capacitance.

Figure 3 is depicts a coiled delay line device 30 having a nominal 1.8 nanosecond delay. Where the path 22 is generally configured in a square shape, the conductive path 32 exhibits a rectangular shape. The input coil 34, output coil 35 and coupling conductor 36 each exhibit a nominal 0.060 inch line width and a 0.070 inch spacing between the coils 34-37 and 35-37''. The coil conductors 37, 37' and 37'' are formed with a nominal 0.230-inch line width and a 0.100-inch spacing between the coils 37, 37' and 37''.

Figure 4 depicts another coiled delay line device 40 having a nominal 4.25 nanosecond delay. The device 40 is constructed in a folding configuration on a flexible substrate 41. A number of coiled delay line segments 42, each similar to the device 20, are distributed about the surface of the substrate. A longitudinal fold line 43 extends between the segments 42 and terminations 44 are provided at the edges of the substrate 41.

An input coil 45, output coil 46 and coupling conductors 49 exhibit a nominal 0.060-inch line width and a 0.080 inch spacing between the coils 45-47 and 46-47". The coil conductors 47, 47' and 47'' are formed at a nominal 0.150-inch line width and a 0.150-inch spacing between the coils 47, 47' and 47". Plated through vias (not shown) couple terminations 48 to each other in an appropriate fashion.

While the invention has been described with respect to a number of presently preferred delay line devices, the invention can be adapted to a variety of other transmission line circuit components wherein it is desired to obtain a substantially constant operating impedance at frequencies greater than 100 MHz. The geometric configuration of the device's conductor pathway can take any desired form, thus the disclosed coil-shaped delay lines should not be held as limiting. It is also to be appreciated the shaping of the line width and line spacing can be selectively relegated to selected regions of the pathway as opposed all uncoupled regions. It is to be appreciated still other circuit and device constructions may be suggested to those skilled in the art. The scope of the invention should therefore be construed broadly within the spirit and scope of the following claims.

What is claimed is: